c. Amendments to Claims

1 – 7. (canceled)

8. (currently amended) An integrated circuit, comprising:

a substrate having a top surface;

collector, base, and emitter semiconductor layers of a bipolar transistor, the semiconductor layers forming a vertical sequence on the substrate in which intrinsic portions of two of the semiconductor layers are sandwiched between the top surface of the substrate and a remaining top one of the semiconductor layers, the base layer comprising an extrinsic portion that laterally encircles a vertical portion of the top one of the semiconductor layers; and

a dielectric sidewall being interposed between the vertical portion of the top one of the semiconductor layers and the extrinsic portion of the base layer; and

wherein the substrate includes a subcollector that forms an electrical contact for the collector layer, the entire subcollector being located outside of the portion of the substrate that is vertically below part of the base layer.

9. (canceled)

10. (previously presented) The integrated circuit of claim 8, wherein the extrinsic portion of the base layer extends farther away from the substrate than an interface between the top one of the semiconductor layers and the base layer.

11. (canceled)

12. (currently amended) The integrated circuit of claim 8, wherein a part of the extrinsic portion of the base layer is located between the substrate and an ~~the~~ extrinsic portion of the top one of the semiconductor layers.

13. (previously presented) The integrated circuit of claim 12, further comprising a

dielectric layer, a portion of the dielectric layer being located on the extrinsic portion of the base layer and the extrinsic portion of the top one of the semiconductor layers being located on the dielectric layer.

14. (previously presented) The integrated circuit of claim 12, wherein the extrinsic portion of the base layer extends farther away from the substrate than an interface between the top one of the semiconductor layers and the base layer.

15. (canceled)

16. (previously presented) The integrated circuit of claim 8, wherein the top one of the collector, base, and emitter semiconductor layers is epitaxially grown.

17. (previously presented) The integrated circuit of claim 8, wherein the top one of the collector, base, and emitter semiconductor layers is a graded layer.

18. (previously presented) The integrated circuit of claim 8, wherein the top one of the collector, base, and emitter semiconductor layers includes gallium.

19. (previously presented) The integrated circuit of claim 8, wherein the top one of the collector, base, and emitter semiconductor layers includes an InP layer.

20 – 21. (canceled)

22. (previously presented) The integrated circuit of claim 12, wherein the dielectric sidewall has a thickness of 500 to 1500 angstroms.

23 – 24. (canceled)

25. (previously presented) The integrated circuit of claim 14, further comprising a

dielectric layer, a portion of the dielectric layer being located on the part of the extrinsic portion of the base layer and the extrinsic portion of the top one of the semiconductor layers being located on the dielectric layer.

26 – 28. (canceled)

29. (previously presented) The integrated circuit of claim 8, wherein the base layer comprises gallium.

30. (previously presented) The integrated circuit of claim 8, wherein the base layer comprises gallium, indium and arsenic.

31. (currently amended) The integrated circuit of claim 8, wherein the substrate is an ~~a~~ InP substrate.